CLAIMS

The invention claimed is:

1. A method of forming a low electrical resistance metal silicide, comprising:

forming a first metal silicide layer over a substrate, the first metal silicide layer having a melting point higher than 1700°C and being metal-enriched, the first metal silicide layer having a thickness of at least about 50Å and comprise a predominate metal;

forming metal-containing layer directly against the first metal silicide layer; the metal of the metal-containing layer predominately being a metal different than the predominant metal of the first metal silicide; and

after forming the metal-containing layer directly against the first metal silicide layer, converting the metal of the metal-containing layer to metal silicide to convert the metal-containing layer to a second metal silicide layer over the substrate; the second metal silicide layer having a bulk resistance of less than 30 micro-ohms-centimeter.

2. The method of claim 1 further comprising:

prior to converting the metal of the metal-containing layer to metal silicide, forming a silicon-containing layer directly against the metal-containing layer; and

wherein the conversion of the metal of the metal-containing layer to second metal silicide layer comprises incorporation of silicon from the silicon-containing layer into the second metal silicide layer.

3. The method of claim 2 wherein the first metal silicide layer is formed on a non-silicon-containing electrically conductive material.

4. The method of claim 2 wherein the silicon-containing layer is formed to a thickness of at least about 400Å.

5. The method of claim 2 further comprising incorporating the second metal silicide layer into a bitline.

6. The method of claim 1 wherein the predominate metal of the first metal silicide layer is selected from the group consisting of Hf, Mo, Ta, and W.

7. The method of claim 1 wherein the first metal silicide layer consists essentially of $TaSi_x$, where x is greater than 0 and less than or equal to 2.

8. The method of claim 1 wherein the predominate metal of the metal-containing layer is selected from the group consisting of Ti, Zr, Sc, Y, Co, Ni, Pd, Pt and Ir.

9. The method of claim 1 wherein the metal-containing layer consists essentially of Ti.

10. The method of claim 1 wherein the first metal silicide layer has a thickness of from about 50Å to about 200Å.

11. The method of claim 1 wherein the metal-containing layer has a thickness of from about 50Å to about 500Å.

12. The method of claim 1 wherein the first metal silicide layer has a thickness of from about 50Å to about 200Å, and wherein the metal-containing layer has a thickness of from about 50Å to about 500Å.

13. The method of claim 1 further comprising forming a layer comprising silicon directly against the metal-containing layer prior to the converting.

14. The method of claim 1 further comprising forming a layer consisting essentially of silicon or conductively-doped silicon directly against the metal-containing layer prior to the converting.

15. The method of claim 14 further comprising forming a silicon nitride cap over the layer consisting essentially of silicon or conductively-doped silicon during the converting.

16. The method of claim 14 wherein the substrate comprises silicon, and wherein the first metal silicide layer is formed directly against the silicon of the substrate.

17. A method of forming metal silicide comprising metal from one or more of Groups 3, 4, 8, 9 and 10 of the periodic table, the method comprising:

forming a first metal silicide layer over a substrate, the metal of the first metal silicide layer predominately being a refractory metal, the first metal silicide layer having a thickness of at least about 50Å;

forming a metal-containing layer directly against the first metal silicide layer; the metal of the metal-containing layer predominately being from one or more of Groups 3, 4, 8, 9 and 10 of the periodic table and being different than the predominate refractory metal of the first metal silicide layer; and

after forming the metal-containing layer directly against the first metal silicide layer, converting the metal of the metal-containing layer to metal silicide to convert the metal-containing layer to a second metal silicide layer over the substrate.

18. The method of claim 17 wherein the first metal silicide layer is metal-enriched, at least prior to the conversion of the metal-containing layer.

19. The method of claim 17 wherein the predominate refractory metal of the first metal silicide layer is selected from groups other than Groups 3, 8, 9 and 10 of the periodic table.

20. The method of claim 17 wherein the predominate refractory metal of the first metal silicide layer is selected from the group consisting of Hf, Cr, Mo, Nb, Ta, V and W.

21. The method of claim 17 wherein the predominate refractory metal of the first metal silicide layer is selected from the group consisting of Hf, Mo, Ta, and W.

22. The method of claim 17 wherein the first metal silicide layer consists essentially of MSi_x, where x is greater than 0 and less than or equal to 2, and where M is one or more metals selected from the group consisting of Hf, Mo, Ta, and W.

23. The method of claim 17 wherein the first metal silicide layer consists essentially of $TaSi_x$, where x is greater than 0 and less than or equal to 2.

24. The method of claim 17 wherein the predominate metal of the metal-containing layer is selected from the group consisting of Ti, Zr, Sc, Y, Co, Ni, Pd, Pt and Ir.

25. The method of claim 17 wherein the metal-containing layer consists essentially of Ti.

26. The method of claim 17 wherein the first metal silicide layer has a thickness of from about 50Å to about 200Å.

27. The method of claim 17 wherein the metal-containing layer has a thickness of from about 50Å to about 500Å.

28. The method of claim 17 wherein the first metal silicide layer has a thickness of from about 50Å to about 200Å, and wherein the metal-containing layer has a thickness of from about 50Å to about 500Å.

29. The method of claim 17 wherein the substrate comprises silicon, and wherein the first metal silicide layer is formed directly against the silicon of the substrate.

30. The method of claim 17 further comprising forming a layer comprising silicon directly against the metal-containing layer prior to the converting.

31. The method of claim 17 further comprising forming a layer consisting essentially of silicon or conductively-doped silicon directly against the metal-containing layer prior to the converting.

32. The method of claim 31 further comprising forming a silicon nitride cap over the layer consisting essentially of silicon or conductively-doped silicon during the converting.

33. The method of claim 17 wherein the converting comprises exposing the metal-containing layer and the first metal silicide layer to a temperature of from about 600°C to about 900°C for a time of at least about 30 seconds.

34. The method of claim 17 further comprising incorporating the second metal silicide layer into a wordline of an integrated circuit.

35. The method of claim 34 wherein the wordline has a width of less than or equal to 0.25 micrometers.

36. The method of claim 34 wherein the wordline has a width of less than or equal to 0.15 micrometers.

37. The method of claim 34 wherein the wordline has a width of less than or equal to 0.11 micrometers.

38. The method of claim 17 further comprising incorporating the second metal silicide layer into a bitline of an integrated circuit.

39. The method of claim 38 wherein the bitline has a width of less than or equal to 0.25 micrometers.

40. The method of claim 38 wherein the bitline has a width of less than or equal to 0.15 micrometers.

41. The method of claim 38 wherein the bitline has a width of less than or equal to 0.11 micrometers.

42. A method of forming titanium silicide, comprising:

forming a metal silicide layer over a substrate, the metal silicide layer consisting essentially of MSi_x where x is greater than 0 and where M is one or more metals other than titanium, the metal silicide layer having a thickness of at least about 50Å;

forming a titanium-containing layer directly against the metal silicide layer; and

after forming the titanium-containing layer directly against the metal silicide layer, converting the titanium to titanium silicide.

43. The method of claim 42 wherein M is one or more of Hf, Mo, Ta and W.

44. The method of claim 42 wherein M is Ta.

45. The method of claim 42 wherein the metal silicide layer has a thickness of from about 50Å to about 200Å.

46. The method of claim 42 wherein the titanium-containing layer has a thickness of from about 50Å to about 500Å.

47. The method of claim 42 wherein the substrate comprises silicon, and wherein the metal silicide layer is formed directly against the silicon of the substrate.

48. The method of claim 42 further comprising forming a layer consisting essentially of silicon or conductively-doped silicon directly against the titanium-containing layer prior to the converting.

49. The method of claim 48 wherein the substrate comprises silicon, and wherein the metal silicide layer is formed directly against the silicon of the substrate.

50. The method of claim 42 wherein the converting comprises exposing the titanium-containing layer and the metal silicide layer to a temperature of from about 600°C to about 900°C for a time of at least about 30 seconds.

51. The method of claim 42 further comprising incorporating the titanium silicide into a wordline of an integrated circuit.

52. The method of claim 51 wherein the wordline has a width of less than or equal to 0.25 micrometers.

53. The method of claim 51 wherein the wordline has a width of less than or equal to 0.15 micrometers.

54. The method of claim 51 wherein the wordline has a width of less than or equal to 0.11 micrometers.

55. The method of claim 42 further comprising incorporating the titanium silicide into a bitline of an integrated circuit.

56. The method of claim 55 wherein the bitline has a width of less than or equal to 0.25 micrometers.

57. The method of claim 55 wherein the bitline has a width of less than or equal to 0.15 micrometers.

58. The method of claim 55 wherein the bitline has a width of less than or equal to 0.11 micrometers.

59. An integrated circuit supported by a semiconductor substrate, comprising:

a first metal silicide layer over the semiconductor substrate, the first metal silicide layer being predominately MSi_2 where M is one or more metals, the first metal silicide layer having a thickness of at least about 50Å; and

a second metal silicide layer directly against the first metal silicide layer, the second metal silicide layer being predominately QSi_2 where Q is selected from Groups 3, 4, 8, 9 and 10 of the periodic table, wherein the metals of Q are different from the metals of M, and wherein the second metal silicide layer has a thickness of at least about 100Å.

60. The integrated circuit of claim 59 wherein M is one or more of Hf, Mo, Ta and W.

61. The integrated circuit of claim 59 where the first metal silicide layer consists of $TaSi_2$.

62. The integrated circuit of claim 59 wherein Q is one or more of Ti, Zr, Sc, Y, Co, Ni, Pd, Pt and Ir.

63. The integrated circuit of claim 59 wherein Q is Ti, and wherein the second metal silicide layer consists essentially of $TiSi_2$.

64. The integrated circuit of claim 59 wherein the first metal silicide layer has a thickness of from about 50Å to about 500Å.

65. The integrated circuit of claim 59 wherein the second metal silicide layer has a thickness of from about 100Å to about 1000Å.

66. The integrated circuit of claim 59 wherein the first and second metal silicide layers are within a wordline.

67. The integrated circuit of claim 66 wherein the wordline further comprises a first layer of conductively-doped silicon beneath the first metal silicide layer and a second layer of conductively-doped silicon over the second metal silicide layer.

68. The integrated circuit of claim 66 wherein the wordline has a width of less than or equal to 0.25 micrometers.

69. The integrated circuit of claim 66 wherein the wordline has a width of less than or equal to 0.15 micrometers.

70. The integrated circuit of claim 66 wherein the wordline has a width of less than or equal to 0.11 micrometers.

71. The integrated circuit of claim 66 wherein the wordline has a width of less than or equal to 0.11 micrometers, wherein the second metal silicide consists essentially of $TiSi_2$, and wherein the second metal silicide has a resistance of less than or equal to about 20 micro-ohms-cm.

72. The integrated circuit of claim 66 wherein the wordline is within a DRAM array.

73. An electronic system comprising the DRAM array of claim 72.

74. The integrated circuit of claim 59 wherein the first and second metal silicide layers are within a bitline.

75. The integrated circuit of claim 74 wherein the bitline has a width of less than or equal to 0.25 micrometers.

76. The integrated circuit of claim 74 wherein the bitline has a width of less than or equal to 0.15 micrometers.

77. The integrated circuit of claim 74 wherein the bitline has a width of less than or equal to 0.11 micrometers.

78. The integrated circuit of claim 74 further comprising a layer of conductively-doped silicon over and directly against the second metal silicide layer.

79. The integrated circuit of claim 74 wherein the bitline has a width of less than or equal to 0.11 micrometers, wherein the second metal silicide consists essentially of $TiSi_2$, wherein the first metal silicide consists essentially of $TaSi_2$, and wherein the second metal silicide has a resistance of less than or equal to about 20 micro-ohms-cm.

80. The integrated circuit of claim 74 wherein the bitline is within a DRAM array.

81. An electronic system comprising the DRAM array of claim 80.